PCC activities overview

Gyorgy Balazs, Havard Bjerke,
Andreas Hirstius, Sverre Jarp, Andrzej Nowak

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Multi-threading activities (1)

- **Third CERN/Intel multi-threading and parallelism workshop, Spring 2008**
  - Collaboration with Technical Training to reduce administrative burden and streamline the class with other Technical Training activities
  - 1 day lectures, 1 day hands-on labs
  - 6 lecturers (1 from Intel, 5 from CERN)
  - We continue to enjoy a high level of satisfaction amongst the participants
- **Next workshop: Fall 2008 (11-12 Nov)**
- **The course is still FREE!**

Multi-threading activities (2)

- **Major advanced in Geant4 parallelization (with Northeastern University, MA, USA)**
  - Xin Dong from NEU a summer student at CERN
  - Geometry entirely multi-threaded
- **The collaboration with the PH R&D project is advancing, but there are no specific results yet**
- **HLT track finder / fitter (see later slides)**
- **Ct review, testing, benchmarking**
- **Jeff Arnold (Intel compiler expert) has just arrived for two months (sabbatical)**
  - memory usage study in multi-threaded apps

Compiler activities

- **Intel ICC 11.0 beta compilers tested**
  - Compared to GCC 4.3.0
  - Conclusive tests
  - New incidents opened after several minor regressions were found
- **New snippet developed by William Romero (openlab summer student)**
  - To be added to the openlab test suite
- **In-order compiler scheduling studies to cover Atom as well (see later)**

Thermal efficiency

- **CERN's energy efficiency paper used as a base for a whitepaper at Intel**
  - Published on the Intel website on the day of LHC launch (http://download.intel.com/products/processor/xeon5000/CERN_Whitepaper_r04.pdf)
- **Gyorgy Balazs has a report ready on individual component power consumption**
  - Focus on Harpertown systems

Performance monitoring (1)

- **Continuing perfmon2 tests and developments**
  - additional functionality
  - deployment on test platforms
  - adaptation to CERN needs nearly finished
  - updates for future processors
- **Intel PTU deployment on test systems**
  - Performance monitoring tool based on the VTune module
- **Benchmark collaboration with the HEPiX Benchmarking Working Group**
  - still deciding which SPEC2006 components are suitable for accurate HEP workload representation
  - all_cpp likely to be accepted

Performance monitoring (2)

- **First computer architecture and performance tuning workshop in "test mode" – Spring 2008**
  - Advanced users from CERN invited
  - Positive and encouraging feedback
- **Lecture series invited to the CERN School of Computing 2008**
  - Promoting Intel technologies
- **Next workshop: Fall 2008, October 14th**

Performance monitoring (3)

- **Perfmon2 project continuing on lxbatch machines (production servers)**
  - perfmon2 is running in system-wide mode, collecting data 24/7 in real time
  - negligible performance hit
  - expanded from 5 dual-core Xeon servers to 60 quad-core Xeon servers

Benchmarking (1)

Benchmark Repository

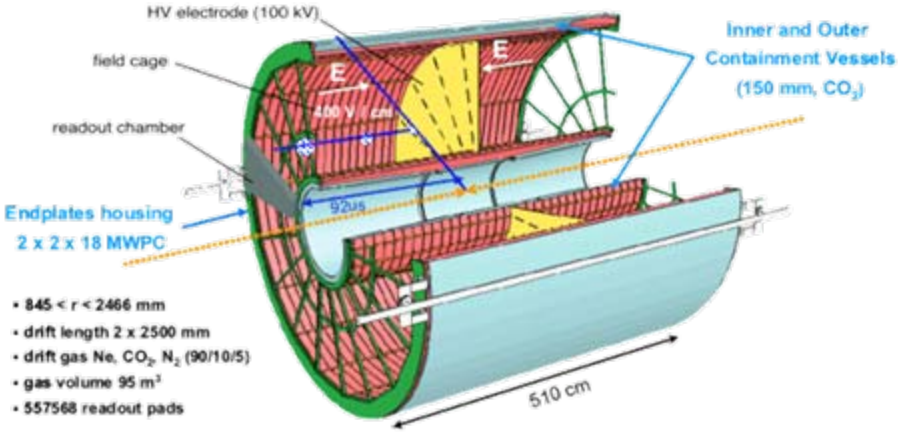
A collection of benchmarks that employ optimization techniques, such as multithreading and vectorization, in order to fully exploit the available resources of CPU architectures.

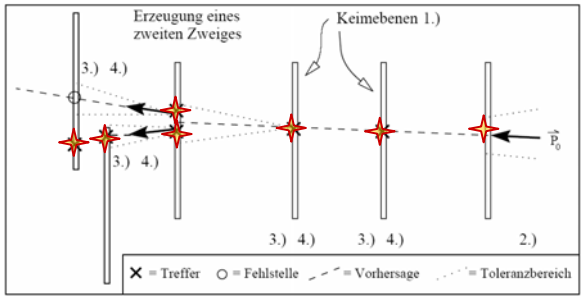
Category	Name	Contact	Optimization techniques
On-line	CBM/Alice track fitting	Ivan Kisel	SSE vector intrinsics, multithreading with Intel Threading Building Blocks
	CBM/Alice: Track finding	Ivan Kisel	SSE vector intrinsics
Accelerator simulation	Tomography	Eric McIntosh	MPI
Theoretical physics	QCD simulation	Martin Lüscher	MPI
Off-line	Geant4 simulation	Gene Cooperman, Northeastern University	TOP-C + underlying system
	ROOT-data compression	Leo Franco	pthreads
	ROOFIT multivariate analysis	Alfio Lazzaro	MPI
	Reconstruction	Unknown	Unknown
Others	SPEC2006 - libquantum	Andreas Hirstius	OpenMP
	TOP500 - Linpack	Andreas Hirstius	OpenMP + MPI
	Game of Life	Ralf Ratering, Intel	SSE vector intrinsics

Benchmarking (2)

High Level Trigger

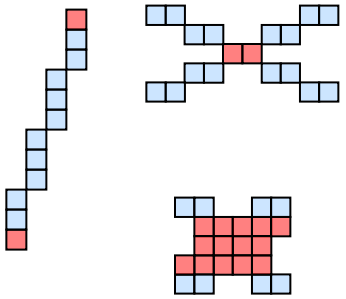
- **Track Finding:** ***Reconstructing particle tracks from events***
  - Under development
- **Track Fitting:** ***Estimate real trajectories from imprecise measurements***
  - Highly thread and SIMD parallel benchmark
- **Collaboration with the ALICE experiment, the CBM experiment and Intel in Bruehl**





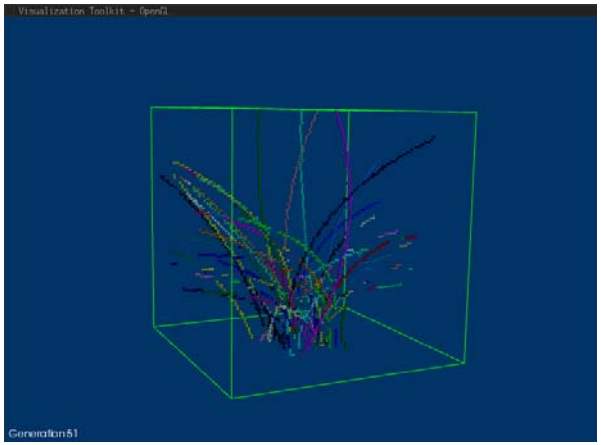
> Cellular Automaton Track Finder

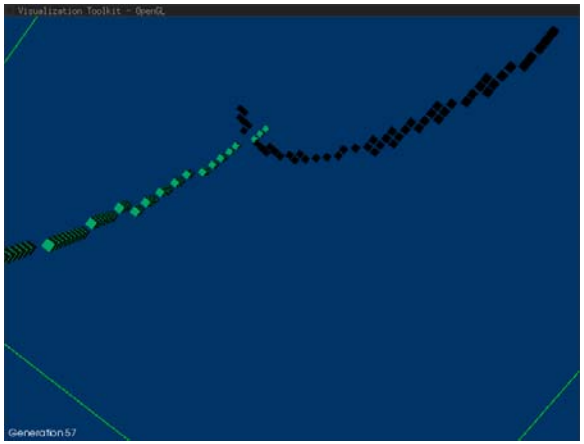
- Interesting CA properties:
  - Simple
  - Local
  - Parallel
- Starvation: No top or bottom neighbour (track endings)
- Overpopulation: (difficult to discern tracks)
  - More than two neighbours
  - An overlap of more than two cells

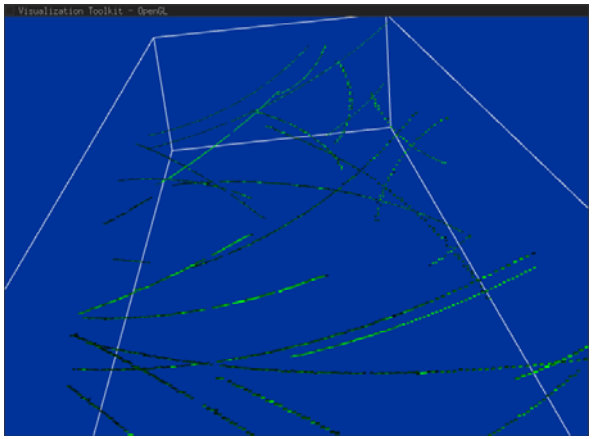


> Track finder developments

- 2D ⟶ 3D
- Intercepting tracks split and produce false positives, which are later merged
- Integration with AliRoot framework provides realistic event simulation







Future Xeons

- **Regular contacts with Intel server group (Tom Garrison's team)**
- **Detailed discussions on next-generation Xeon processors**
  - memory controllers
  - QuickPath technology
  - performance monitoring unit

Atom

- **Board received in early September**
- **Installed by Gyorgy Balazs within 24 hours**
  - scavenged components from other PCs
  - 250 W supply, but the board consumed max 70!
- **Power consumption gotten down to 45W in a typical case, 37W minimum**
  - only a minor fraction of that is the CPU!
- **Compared 2-way Atom to 8-way Xeon in terms of throughput, thermals, consumed power and cost**
  - A paper is in the works